a packet of the serial data in parallel form to one of a plurality of devices associated with data applications.

The above claim broadly encompasses the structure illustrated in Fig. 1 of the subject application, which includes a serial to parallel converter 110 that receives time-division multiplexed serial data (CB_DATA) and provides 8 bit (1 byte) wide parallel formatted data (CDATA) to FIFOs 130-136, which are each associated with an application device. The cited art fails to teach claim 1 as a whole, and, in particular, such a serial to parallel converter.

The Office action relies upon Fig. 3 of Swenson. *See, 11/3/2005 Office action, par. 4.* However, a detailed reading of Swenson clearly reveals that Fig. 3 does not illustrate a serial to parallel converter, but, as Swenson itself recites, "FIG. 3 is a logic diagram of eight parallel-to-serial converter circuits." *See, col. 2, lines 60-62.* The parallel to serial converter circuits of Fig. 3 of Swenson do not disclose or suggest the recited serial to parallel converter of Claim 1.

The Final Office action further states on paragraph 4, lines 4-11, that Swenson teaches a serial to parallel converter having a single serial data input line adapted to receive time division multiplexed (41) serial data from a plurality of data sources (PI(0)-PI(7)) and a plurality of parallel output lines to a plurality of devices associated with data applications (51-58) in Fig. 3. It thus appears that the Examiner is attempting to extract a portion of Swenson's parallel to serial converter circuit and recast it as a serial to parallel circuit arrangement for purposes of reading onto Claim 1. However, a detailed reading of Swenson and application of the Swenson reference to present Claim 1 reveals this piecemeal extraction nevertheless, still fails to teach each of the limitations of Claim 1.

In particular, multiplexer 41 of Swenson is directly coupled to *registers 51-58* of Swenson, which the Office action *equates to the devices coupled to the parallel output* of the claimed *serial to parallel converter.* That is, as part of the parallel to serial conversion of Fig. 3 of Swenson, when 8 bits of each

of 8 parallel bytes have been stored in a RAM 40, multiplexer 41 reads and transmits the stored data to the registers 51-58, one register at a time. Thus, Swenson fails to teach, or suggest, the recited serial to parallel converter of Claim 1, as, in Swenson, the multiplexer 41 multiplexed serial data is directly applied to the structure (51-58) that the Office action equates to the "devices", whereas Claim 1 instead calls for the devices being coupled to the parallel outputs of a serial to parallel converter.

In other words, Claim 1 calls for a serial to parallel converter which has an input that receives the recited multiplexed serial data stream and that then outputs it in parallel form to a plurality of devices. Swenson instead merely shows a multiplexed stream being loaded from a multiplexer 41 directly into registers 51-58.

Thus, the Swenson reference as applied in the present Office action, clearly fails to teach or suggest: (1) a serial to parallel converter; and more particularly, (2) a serial to parallel converter having (a) a single serial data input line adapted to receive time-division multiplexed serial data from a plurality of data sources; and (b) a plurality of parallel output lines that provide a packet of the serial data in parallel form to one of a plurality of devices. In contrast, the multiplexer 41 of Swenson loads the purported serial stream from the multiplexer directly into registers 51-58. The secondary reference of Dally as applied in the Office action adds nothing to correct the deficiencies of Swenson in these regards. Accordingly, as the cited references of record fail to teach each of the limitations of present Claim 1, reconsideration and withdrawal of this 35 USC 103 rejection is requested.

In the event the Examiner does not withdrawal the present rejection, Applicant requests the Examiner clearly and unambiguously identify the specific structure(s) in Fig. 3 of Swenson that are being equated to the recited serial to parallel converter having (a) a single serial data input line adapted to receive time-division multiplexed serial data from a plurality of data sources; and (b) a plurality of parallel output lines that provide a packet of the

serial data in parallel form to one of a plurality of devices, in accordance with MPEP § 706.02(j).

2. A Proper Motivation For Combining The References Is Lacking

The above notwithstanding, the Examiner has not provided a proper motivation for combining the references of Swenson and Dally, absent impermissible hindsight gleaned from Applicant's own disclosure.

To establish a *prima facie* case of obviousness, there must also be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings. *See, M.P.E.P. §706.02(j); see also, In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).* That is, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *See, M.P.E.P. §2143.01; see also, In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).* In the present case, a proper motivation has not been established for combining or modifying the primary reference Swenson with the secondary reference Dally.

Claim 1 recites, in part, "enable logic coupled to each of said plurality of devices and adapted to provide at least one data valid signal that identifies which of said plurality of devices are associated with a particular packet of said time-division multiplexed serial data." The Office action admits that Swenson fails to teach, or suggest, enabling logic that identifies which of a plurality of devices are associated with a particular packet. *See, e.g., 11/3/2005 Office action, par.4, lines 16-18.* The Office action attempts to rely on Dally to remedy this deficiency of the primary reference. In particular, the Examiner argues:

> it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Swenson with the teaching of Dally to provide at least one data valid signal that identifies which of a plurality of devices are associated with a particular packet in order to reduce the pin count

within a switching element through the use of a multiplexer.

This conclusion is completely unsupported in the cited art, and improperly resorts to "hindsight" based upon applicant's own disclosure.

The Swenson reference explicitly states it is concerned with "provid[ing] a converter with a lower transistor count thus reducing the area consumption on an Integrated Circuit." *See, col. 1, lines 34-41.* Dally is concerned with providing high levels of productive processor cycle usage by implementing conditional vector operations. *See, col. 3, lines 40-52.* Neither Swenson nor Dally teaches, or even addresses, reducing pin count. Rather, such motivation is only identified in the subject application itself.

Further, Swenson fails to teach or suggest that productive processor cycle usage represents a problem for parallel to serial converters of the type shown in Fig. 3, as the parallel to serial converter shown in FIG. 3 merely loads and unloads latches responsively to specific clock cycles. Dally likewise fails to disclose the suitability of conditional vector processing for use with the latching system of parallel to serial converters. Accordingly, Applicant submits the Office action improperly relies upon Applicant's own disclosure, and not the art of record, for the purported motivation to combine the references as argued.

Still further, the proposal to modify the primary reference which teaches a *parallel to serial* converter circuit arrangement, by extracting portions of that reference in an attempt to form a *serial to parallel* converter, and then further changing the functionality of that piecemealed portion of the primary reference by somewhere or somehow introducing a "data valid signal that identifies which of a plurality of devices are associated with a particular packet" based on purported "desire to reduce pin count in a switching element through use of a multiplexer" (which motivation is nowhere disclosed or suggested except in Applicant's specification), simply has no basis in fact or logic.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 1, as (1) the cited art fails to teach, or

suggest, each of the recited limitations thereof, and (2) a proper motivation for combining the references as argued is lacking. Applicant also requests reconsideration and removal of the rejections of Claims 3-5 as well, at least by virtue of these claims' ultimate dependency upon a patentably distinct base Claim 1.

With regard to Claim 6, it analogously recites:

> [a] method for transmitting serial compressed data from a plurality of data sources to a plurality of devices associated with data applications, comprising the steps of:
>
> time-division multiplexing the serial compressed data from the plurality of data sources to generate time-division multiplexed serial compressed data onto a single data line;
>
> converting the time-division multiplexed serial data to a packet of parallel data, and outputting said packet of parallel data for receipt by at least one of said plurality of devices associated with data applications; and
>
> providing at least one data valid signal that identifies which of said plurality of devices are associated with said outputted packet of parallel data. (*emphasis added*)

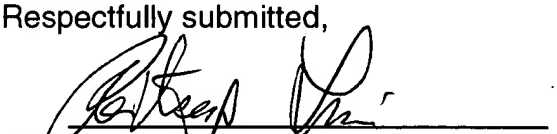
Accordingly, Applicant requests reconsideration and removal of the rejection of Claim 6 as well, for at least the reasons set forth above with regard to Claim 1. Applicant also requests reconsideration and removal of the rejections of Claims 8 and 9 as well, at least by virtue of these claims' dependency upon a patentably distinct base Claim 6.

CONCLUSION

Having fully addressed the Examiner's objections and rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,



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